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GGE Gielen, HCC Walscharts, WMC Sansen - Solid-State Circuits, IEEE Journal of, 1989 - ieeexplore.ieee.org
... Secondly, the explicit representation of **mismatch** terms allows the ... The output **impedance**
is now given by Rj(g2ç1 ... 4. The sym- (5) bolic **simulator** clearly gives ...
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LT Tang, PL So, E Gunawan, YL Guan, S Chen, TT Lie - Power Delivery, IEEE Transactions on, 2003 -
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... struck" dipole receivers in a **simulation** event, along ... this **frequency** is evident in
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... system building as demonstrated by the **simulation** of a ... to that of threshold voltage
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... of γ and the mode **mismatch** parameter K ... the corresponding dark-fringe pattern computed
by the **simulation**. ... At some point the PRC becomes **impedance**- matched where ...
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R Pintelon, L Van Biesen - Instrumentation and Measurement, IEEE Transactions on, 1990 - ieeexplore.ieee.org
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... variations in the **impedance** of the short. ... are also caused by process gradients which
produce device **mismatch**. ... Section 2, the fault **simulator** takes the network ...
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... However, alternative composite structures for **impedance-matching** could he developed
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SYNTHESIS One obvious use of ... stub- networks by means of computer **simulation**. ...
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... account for pos- sible amplifier **impedance mismatch** and biasing ... As regards NPR
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arrays ... the dynamic range, bandwidth, **impedance matching**, and simplili ...

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... that is identical to the design **simulation**. ... test, and connectivity tests including
flying **probes**. ... Weekly **code coverage** analysis (both functional and line ...
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... Signal **Coverage** 121 3.9.2 Performing **Code Coverage** Analysis 121 ... DAC 143 4.6.2 Creating
the **Netlist** 146 4.6.3 ... 5 **Simulation** 153 5.1 Functional **Simulation** 154 5.2 ...
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R Bryant, KT Cheng, A Kahng, K Keutzer, W Maly, R ... - Proceedings of the IEEE, 2001 - ieeexplore.ieee.org
... to a logic-gate-level representation (logic **netlist**) using the ... a single mask set
and **probe** card costs $1 ... **Code coverage** fails to measure the occurrence of event ...
<u>Cited by 20</u> - <u>Web Search</u> - <u>BL Direct</u>

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V Bertacco - 2003 - eecs.umich.edu
... the ability to mix cycle-based and **event-based simulation**. ... design under test are
visited during each **simulation** ... is commonly used in industry is state **coverage**. ...
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<u>Development and Verification of fast C/C++ Models for the Star12 Micro Controller</u> - <u>group of 2</u>
<u>»</u>
J Schlosser - schlosser.info
... between the functions is no longer **event-based**, but a ... this level a first performance
simulation is possible. ... **Code** optimizations take place as well as adoptions ...
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<u>verificationavenue</u> - <u>group of 11 »</u>
B Regards - synopsis.com
... designs and provides links to **code** for easy ... of Formality ® 2003 expands datapath
coverage, improves datapath ... performance when the gate level **netlist** has been ...
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<u>A Device-Level FPGA Simulator</u>
JE Hunter III - 2004 - scholar.lib.vt.edu
... 5.4 HelloTile example **code** . . ... is used to create a **netlist** of all internal connections. ...
Unlike JRoute in JBits2.8, ADB provides complete device **coverage** and is ...
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A Evans, A Silburt, G Vrckovnik, T Brown, M ... - Design Automation Conference,
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faster **simulation** or coding ... drastically reduce the overall **verification** effort ...
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H Forsberg, P Bjureus, I Soderquist, P Lamaty, D ... - Digital Avionics Systems Conference, 2004. DASC 04 The
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pre-compiled or not), Tesivectors (**simulation scripts**, generators), Synthesis ...
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... with the circuit description in a **netlist** format and ... a considerably large speed up
in **simulation** time and ... faults produced test sets with high **coverage** of all ...
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S Sarkar, G Subash Chandar - doi.ieeecomputersociety.org
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Robert E. Canright
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Publisher: IEEE Press

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Distortion Under Nonlinear Load-Pull Conditions
G. Vandersteen, P. Wambacq, S. Donnay, F. Verbeyst
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
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Designing complex analog systems needs differentabstraction levels to reduce the overall complexity. Therequired level of abstraction depends on the accuracy andthe purpose of the model. High-frequency amplifier modelscan vary from simple transfer functions for efficient bit-error-rate analysis up to detailed transistor leveldescriptions for accurate load-pull prediction. This paperintroduces a nonlinear black-box model for high-frequencyamplifiers. It extends the linear S-parameter representati ...

3 Reflections of high speed signals analyzed as a delay in timing for clocked logic   ▨
◆ R. E. Canright, A. R. Helland
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This paper develops equations that can extend the performance of high speed digital systems. The equations allow the application of timing analysis to the selection of the minimum series terminating resistor. Use of the minimum terminating resistor minimizes